

**REMARKS**

Reconsideration and allowance are requested.

The subject matter of claims 5-8 is incorporated into claim 1; the subject matter of claims 15-18 is incorporated into claim 7; and the subject matter of claims 25-28 is incorporated into claim 13.

Regarding the antecedent basis objections raised with respect to claims 9, 19, and 29, the amendments to claims 1, 7, and 13 provide the necessary antecedents. Withdrawal of these objections is appropriate.

Regarding the statutory subject matter objection raised with regard to claim 13, that claim now recites "A computer program product stored on a computer-readable storage medium ...." Applicant respectfully submits that this amendment overcomes the Examiner's specific objection regarding transmission media. Withdrawal of this rejection is requested.

Claims 1-7, 10-17, 20-27, and 30 stand rejected for anticipation based on U.S. patent 6,907,598 to Fraser. This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Fraser fails to satisfy this rigorous standard.

Claims 1, 7, and 13 now incorporate the subject matter of claims 8, 18, and 29, respectively. As the Examiner observes, Fraser lacks that subject matter. However, the Examiner rejects claims 8, 9, 18, 19, 28, and 29 as obvious in view of Fraser. The Examiner's

obviousness rejection is based on an Official Notice position regarding exception handling circuits. Applicant respectfully requests that if the Examiner maintains this rejection, the Examiner supply a prior art reference to support this position, particularly in the context of a data processing apparatus that includes both a program counter and a block counter register.

In addition, the Examiner should understand that the claimed exception handling is not simply conventional exception handling. Rather, a block count value, which is an offset from the beginning of a macro block of two or more instructions, is saved. Advantageously, that block count value only requires a few bits, which means it can be readily added to the data that is saved when the exception occurs. The macro block location itself does not need to be stored because it can be derived from the execute block instruction and the normal program counter value.


Another difference from Fraser's Echo instruction is the claimed execute block instruction encodes the size of the block—the claimed block length field—rather than the number of instructions. Claim 1 recites, for example, "said block of two or more instructions containing a number of program instructions *specified by a block length field* within said executed block instruction." Since instructions can vary in length, the claimed block-length field allows the prefetch hardware to immediately redirect fetches of the main program flow after the end of the execute block instruction without having to first decode the instruction flow and count the number of instructions executed, which is what Fraser must do in the Echo situation.

The application is in condition for allowance. An early notice to that effect is respectfully submitted.

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Respectfully submitted,

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